NO (3 pages)

WOODY AND
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HOW ARE YA?

PLEASE SEND
THE LIST OF TOOLS
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TALK TO YA
BY PHONE
TOMORROW

VIDEO ARCHITECTURES - APPROACHING REAL TIME

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SUMMARY

Overview of video architectures that are specialized toward real time interaction and response. Issues of Analog vs. digital techniques, and resolution/speed tradeoffs are discussed. Novel systems are described that achieve real time performance.

REAL TIME VIDEO

Some working definitions of Video time-scales are :

Real Time

Real time refers to visual tools that generate pictures fast enough to accurately portray movement and instantaneous interaction of the machine with an image. This speed is commonly locked to the transmission or recording Frame rate :
24 frame/sec. for film,
29.97 frames/sec. NTSC video, and
25 Frames/second for European video (PAL, SECAM). Sequences of frames at rates greater than 15 per second, give a reasonable illusion of smooth movement.

B) Interactive Time

Interactive Time refers to a performance level where actions generate visible results which perceptually can be connected to their stimulus. Echoing a character to a display, tracking of a cursor, and responding to a command are operations working in Interactive time. Roughly this speed is from 1/15 of a second to 5 seconds.

C) Animated Time

Animated Time - Animated time will inherit all speeds slower than a human tolerance for interaction : between 5 seconds to 1 day/frame. Full movement is perceptible only in its aggregate form, after accumulating the entire sequence of frames. Time lapse photography is an example of animated time; but frame by frame video recorders and optical disks are seeing increasing usage in computer graphic animation.

THE VIDEO SIGNAL

Achieving real time video involves 'running alongside' the video signal to maintain adequate bandwidth. The relation of active video time to blanking time, gives the proportion of overhead : how much time is spent synchronizing verses the amount of time for signal transmission. The use of two fields displaced 262.5 lines apart to achieve interlace, causes images to be displaced in time by 1/60 of a second. Processing of motion and vertical features need to account for the odd lines scanned in one field, with the even lines following 1/60 of a second later, in the other field.

Gross field/frame related changes must be completed in the Vertical Blanking interval to prevent 'flashing' the screen with partially complete operations. Color changes and input switching are commonly locked to the vertical interval. (Figure 1)

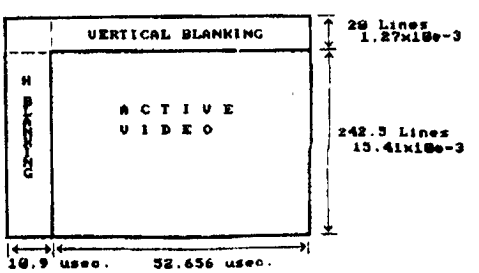

Figure 1. NTSC VIDEO FIELD TIMING

ANALOG and DIGITAL PROCESSING

For processing of video images, analog and digital techniques are in everyday use. Certain processing modules appear frequently in video equipment : the video amplifier, adder, multiplier, electronic switch, and keyer, are some examples. Module operation is governed by numerous control inputs. These controls can be static (fixed) or dynamic - changing at speeds up to the video rate. In the analog domain the controls are voltages and currents, while in the digital domain they are digital control codes.

The Digital components require specifying the maximumum clock rate, the number of bits of resolution, and the number base and arithmetic exceptions (saturating/nonsaturing addition etc.). The examples shown are synchronous, having a clock to line up data marching through the modules. The Analog components perform 'saturated' arithmetic, and have bandwidth 'rolloff' and low level noise which limits their resolution.

PROCESSING MODULES

Video Amplifier -
Analog : Hi-freq OP AMP
Digital : Multiplier

Voltage Contrplled Video Amp -
Analog : Video rate multiplier/ Programmable gain amp
Digital : Multiplier with second input as control

Comparator - High Gain Video Amp operating in differential mode. It achieves a two-state output : a '1' if IN_1 > IN_2 or a '0' if IN_2 < IN_1. Useful in flash A/D converters and KEY generation.

Electronic Switch - one of many inputs are routed to a single output by a control signal. A Video rate switch is a 'Hard Edge Keyer', with the control input being the KEY. (Figure 2)

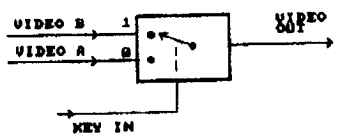

Figure 2. HARD EDGE KEYER

Delay Element -
Analog : Cable Delay, Amplifier delay, tapped delay line, quartz delay line, Video tape delay line.
Digital : reclocking register, shift register (arbitrary length) FIFO, Line buffer, Field buffer, Frame buffer, Magnetic Video Disk Optical Video disk , Laser Video Disks.

Adder - Provides the sum of two or more inputs
Analog : video Op-Amp
Digital : two input adder

Boolean Logic - uniquely digital functions : OR, AND, EXOR and Complement

ALU (Arithmetic Logic Unit)
Digital : processes the additive and Boolean functions

Priority Encoder :
Digital : Ouput = binary encoded number of the greatest numeric input

Multiplier : Output is the product of the two inputs

Memory Elements -
Analog : Hybrid CCD delay line, CCD image sensor/memory
Digital: Lookup tables, Frame/field buffer

Ancillary Processing Components

Phase Locked Loops : aligns the clock phase of internal clocks to external sync. Used in gen-lock (Sync Generator lock) to match the external timing to internal address/timing.

A/D converter - converts analog voltage levels to digital codes

D/A converter - converts digital video to analog outputs

DC restoration - Analog correction of 'AC' coupling in video

Color Encoders / Color Decoders - converts R,G,B signals to/from a composite form for transmission or recording.

DIGITAL VIDEO AMPLIFIER

The digtital video amplifier is a 2 input Multiplier, with Input_1 the Video-In, and Input_2 = Gain. The multiplier is either an LSI circuit commonly (8 to 16 bits), or composed from programmable memories (PROMS, EPROMS) with fixed gains. (Figure 3).

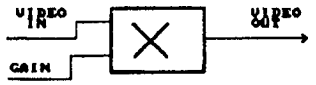

Figure 3. VARIABLE GAIN VIDEO AMPLIFIER

THE UBIQUITOUS LOOKUP TABLE

Unique to digital video processing is the extensive usage of memory as a processing element. The ability to delay, store, retrieve data, and generate functions are major applications of memory components. One example is the Lookup table or Mapping memory. The Lookup table is a fast clocked memory which translates data on input, to new data on its' output : Output = F (Input). A fixed table is 'hardwired' or programmed to one set of values, while Read/write lookup tables allow programming a variety of functions. While the most general of processing elements, its limitations stem from the number of input bits and output bits which can be placed in one memory array. The greater the number of entries (addresses), the larger the memory; the longer it takes to load or modify. Some contend that the frame buffer is a large lookup table with 2 inputs : an X-Display address and a Y-Display address. For a 512H by 512V size frame buffer this needs 256K entries, not conveniently loaded in one Video blanking interval (1.3 milliseconds).

Color Lookup Table (Pseudo-Color)

Given a digital video data stream, the input data often 4-12 bits 'deep' is translated through a set of 3 read/write lookup tables. Each table is assigned to an output channel; one to red, one to green and one to blue. The output of the tables are routed to Video speed Digtial to Analog Converters (D/A's) and sent to an R,G,B monitor or NTSC color encoder (Figure 4). The tables set the correspondence between the monochrome input and colors at the output. If all 3 tables are set to unity (a ramp), the monochrome input generates a monochrome output. If specific entries are set to different values in each table, a color will be output when the table entry shows up on the video stream.

If the input to the table comes from a frame buffer scanned out at display rate, the tables connect color to frame buffer data. In computer graphic Paint systems, operations are perfromed on the frame buffer with a corresponding color map, tagging color to pixel data.

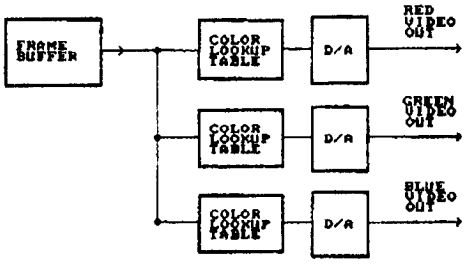

Figure 4. PSEUDO COLOR LOOKUP TABLES

Color-Map Rotation :

An interesting effect used in paint systems is the 'rotation' of the color map entries. The entries are bubbled up through the table by copying the entries from locations below to one location above. The top entry is move to the bottom of this 'Map ribbon'. With a sequential grey scale fluid movement, and Marquis effects simulated. This operation must be performed at frame rate, in the vertical blanking interval to prevent 'flashing' the screen while changing the table entries.

Remapping Memory

Another use is to map input to output through a desired function. The input marches through the memory and arrives at the output one clock later, mapped through a new function. This function can be exponential linear, clustered numbers, or singular entries. (Figure 5)

Figure 5. REMAPPING MEMORY

Gamma Correction - Fixed functions are used as gamma correction tables placed before output D/A converters to correct for the 'intentional' non-linear response of video monitors.

Thresholding - By turning specific entries in the table OFF, with the remainder set to a grayscale, only designated gray values make their way through the table. This is useful to view restrained section of the input grayscale, or to mask out unwanted gray values.

Intensity Compensation - If an input signal/image has a nonuniform grayscale response caused by incorrect exposure or brightness offset, the table is set to the inverse function, effectively cancelling out the input error.

Selector - since the table maps Address to Data, certain address bits can be masked off through the table, eliminating them from the mapping function. This eliminates the contribution of groups of gray levels, 'Masking' or turning them off. If the input is from the frame buffer, bit plane masking can be achieved in the output lookup table.

Control Table - As a control table, instead of greyscale values being mapped into other grayscale values; the output of the table is used to control other hardware. This control information corresponds to the grayscale value of each pixel, allowing each pixel gray value to have an independent function assigned to it. Control of input selectors, ALU functions, and destination controls are applications for control tables. (Figure 6)

Figure 6. CONTROL TABLE

FRAME BUFFER

The frame buffer is a large block of memory applied to storage of the entire video frame. When the memory is time locked to the horizontal and vertical sync, the output pixels form a stable pattern for display. Allocation of memory cycles, input/output data and address selection are essential to achieve full speed video rates. Time must be allocated for 'refresh' when using dynamic memories to maintain data integrity.

The number of inputs and outputs are the PORTS of the frame buffer. For a given memory bandwidth memory, the fight for memory bandwidth by each port is a major concern of system performance. For a display related frame buffer one Read Port is dedicated to the screen access. To ship information into the buffer a Write Port must be dedicated.

Single Cycle Memory

In a single cycle memory system (the memory bandwidth can only sustain one access per pixel), the write function can only occur while Not reading. To prevent interruption of the screen display (resulting in the distasteful flashing or glitching of pixels), access must be limited to the video blanking intervals.

Video Digitizing and Read/Write Access

Curiously the need for bidirectional access to the frame buffer is often ignored. Early frame buffers for computer graphics left out provisions to 'READ BACK' the images just written. The data went in, reached the display but could not be extracted as pixel data by the computer port. Similar ommisions are found in Lookup tables that are Write-Only. This ommission was provoked by building 'Display-Only' devices, that generated line drawings and boxes. With greyscale image generation and retrieval, the Read and Write port should always be present. What goes in must come out.

The other side most often ignored in frame buffers is video input capability. If the memory can be scanned out at video rate, it can also be 'scanned in' in real time (video digitizing). In a single port

system the output can 'echo' the input video giving an output while digitizing, useful for adjusting or focusing the input source. The video input is received from the video rate A/D converter. To digitize real time video, the display system MUST GEN-LOCK, to align its internal timing to the external video source. (Figure 7)

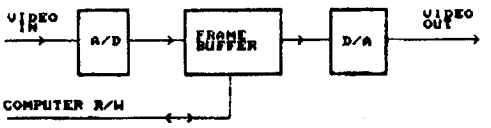

Figure 7. Video Digitizing

In a read/modify write frame buffer, the image pops out one frame later than it's input video. This delay is useful in image accumulation, color noise reduction, edn other frame comparison operations. A minimum set of ports for a real time video buffer are :

1) A real time video input Port (Write Port)
2) A real time video output Port (Read Port)
3) A computer Write Port and Readback Port

FEEDBACK PROCESSING

Given a delay element and a processing element, feedback processing is possible. A portion of the output data is rerouted and combined with the input. This technique is employed in recursive digital filters; and with the delay set to one frame - time and motion effects can be processed.

Configuration -

Video_In routes to one input of an ALU, output of the ALU goes to digitizing input of the frame buffer, output of frame buffer runs to the second input of ALU. The input is compared against the output, with the result of the comparison selecting the ALU function. Variations on this configuration perform :

1) Frame Accumulation - (Noise Reduction, Frame averaging) The input is added to the previous frame, scaled by one half, then rewritten to the frame buffer. This is run for N frames. Stationary low light level images will be accumulated into the frame buffer. If the feedback gain and input gain are adjusted this configuration will perform noise reduction. (Figure 8)

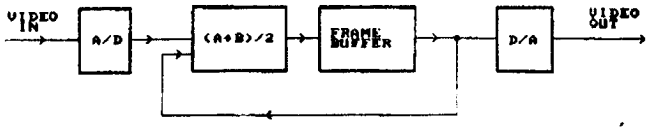

Figure 8. - Frame Accumulate

2) Motion Detection - (Motion Detection, Noise accumulation) The control selection is set to two ALU functions. A comparator is used to select the ALU function, based on the difference between the current input and the previous frame. This writes only changing information back into the frame buffer, if the input video exceeds a certain THRESHOLD. Levels below the threshold are considered noise and are not accumulated. (Figure 9)

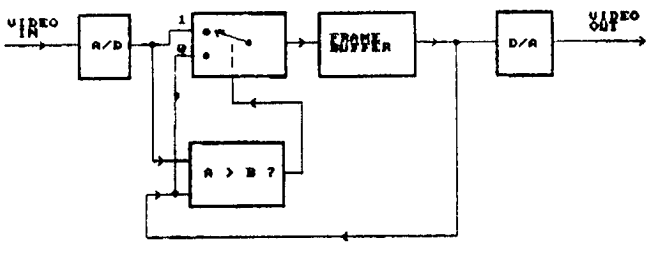

Figure 9 - Motion Detection

SCAN PROCESSOR

A unique real time video processor is the scan processor. Its principle of operation is to intercept the sweep signals of a display monitor and modulate these signals with control voltages. An Analog example is the Rutt/Etra scan processor, with a simplified block diagram shown in Fig. 10. The raster is manipulated by control voltages feeding two chains of four-quadrant multipliers and a summing amplifier, placed between the H and V ramp

generators, and their corresponding deflection yokes. The video signal runs through a multiplier followed by a summing amp for intensity and brightness control.

The control voltages are driven either from 'static' voltage sources or from Function Generators locked to : Horizontal sync, Vertical sync, or themselves ('freerunning'). AM and FM control allow cascading these control signals. Images are 'rescanned' by a camera facing the modulated monitor, with optical effects achieved by placing objects between the rescan camera and the monitor.

The raster's size, position and intensity can be modulated through voltage control signals. The ability to modify the underlying scan process along with the video signal are unique properties of the scan processor.

The need for intensity compensation of small rasters, resolution loss due to the rescan process, and the difficulty of achieving repeatable raster movement using Analog control generators have been some of the shortcomings of this scan processor. Digital control signals run through D/A converters, can simplify the control structure and improve repeatability.

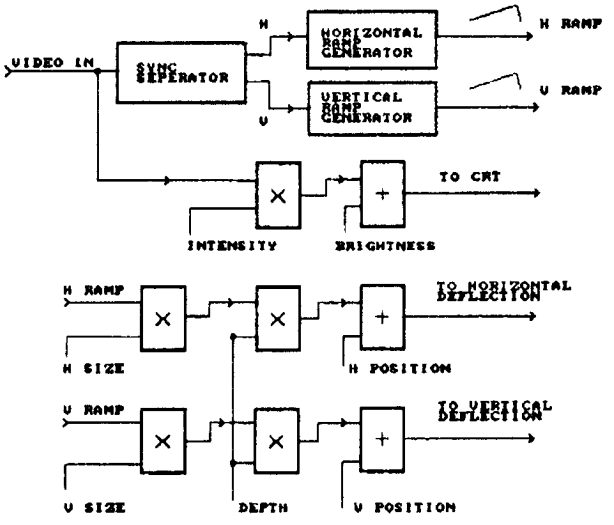

Figure 10. RUIT/ETRA SCAN PROCESSOR SIMPLIFIED BLOCK DIAGRAM

PROCESSING AMPLIFIER

Composite processing of the video signal is exemplified by the aptly named Video Processing Amplifier (or PROC AMP). The Proc Amp's primary function is to cleanse the composite video signal of aberrations injected after routing through a long chain of video components. The Proc Amp seperates the Luminance, Chrominance, and Sync information; only to place them back together with independent control of their levels. The luminance brigthness (Black Level), its contrast (Luminance Gain), Detail (Edge enhancement), White and Black clipping (to inhibit overshoot/ undershoot) are adjustable through Voltages driven from front panel controls. The chroma infromation is extracted (by its 3.579545 MHZ frequency) and the Saturation (GAIN)) and Hue (Phase) are adjustable. The sync signal is further 'Regenerated' to reconstruct any vertical or horizontal sync distortions, with a new color Burst signal inserted on the back porch for the chroma reference phase. A reconstructed video signal is built up through control of its 'component' parts.

The Proc amp while designed for video correction can also become the active component of a video effect unit. Substituting front panel control voltages, with video rate control voltages, the Colorizer is born. The Colorizer's basic function is the insertion of color onto a monochrome signal. The video signal thus emerges as both an image source and a control source for selecting color. The generation of the video image, directly from signals or voltages is termed 'Direct Video Synthesis'. Stephen Beck, Dan Sandin, Dave Jones, Bill Hearn, Eric Siegel, and George Brown are have each developed video processors, whose images are generated and controlled from video and non-video rate signals.

COLORIZER

The majority of colorizers are expansions upon the Proc Amp with the controls derived from the luminance signal. The distinction between a composite black and white signal and a composite NTSC color signal is the presence of the 3.579545 MHZ subcarrier and its reference Burst. Given a black and white signal, the burst and subcarrier is synthetically generated, converting it into a color signal. The method of subcarrier generation distinguishes different breeds of colorizers. Three distinctions will be made - the modulation based colorizer the 'slicing' threshold based colorizer, and the NTSC encoder/colorizer.

Direct Subcarrier Modulation Colorizer

An example of a modulation' colorizer is the Eric Siegel Colorizer shown in block form in Fig 11. A monochrome signal is input, filtered of extraneous 3.58 MHZ components, its luminance component is 'detail enhanced' then run to a chroma Phase SHift Modulator. This modulator links the contrast component of the input to the output Hue . This phase shifter, is a two stage circuit enabling greater than 360 degree rotations in hue space from a black to white video excursion. The amount of phase shift and its polarity is selected through front panel controls, as well as starting phase and saturation. This device is representative of the Direct Subcarrier Modulation colorizer.

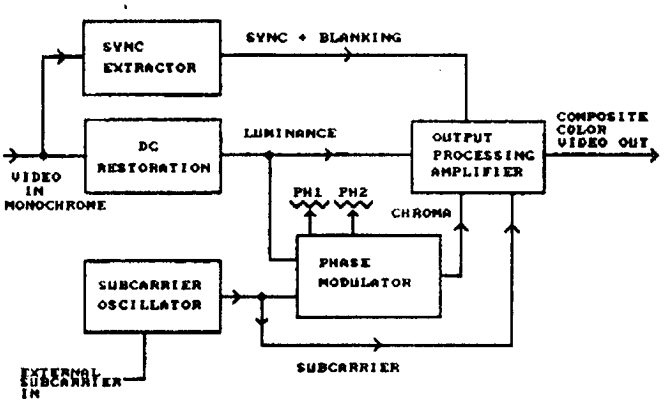

Fig. 11 - Eric Siegel Colorizer Simplified Block Diagram

Luminance Classifying Colorizer

The Threshold based colorizer, classifies luminance into multiple bands, with independent control within each gray region. Two examples of this are the Bill Hearn EAB colorizer, and the David Jones multiband colorizer.

The luminance component is filtered then shipped to a bank of comparators. Each comparator detects a luminance threshold and combines to form 'bands' of gray, which gate on a set of chroma/luma controls. If the thresholds are non-overlappping, the controls operate independently to set brighness, saturation, hue, and contrast; in each gray band.

NTSC Encoder / Colorizer

This colorizer is based around the RGB to NTSC color encoder, as the active color encoding element. The R,G,B camera inputs are exchanged with other control signals, some of them at video rates. The use of the NTSC encoder restrains the output, to be within the bandwidth restrictions of NTSC. Correct observation of these limitations helps avoid 'color smear', and lost detail in the encoded color picture. If the 3 inputs are from a digital video source we arrive at the Pseudo Color colorizer.

Digital Pseudo Color Colorizer -

The number of classfying bands has been limited practically to 10 analog bands. Beyond this, the number of control points becomes inordinately large and unwieldy to control. Interestingly 'Flash A/D converters' consist of the same classifying arrangement : a bank of comparators compare the input video against a chain of voltage references. The references are equally spaced, and not independently adjustable. The A/D further converts the detected levels into an encoded binary value before output. This 'digitized' video signal is passed through to a triple set of lookup tables and D/A converters, then to the RGB to NTSC color encoder. This digital method simulates many of the linear functions of the analog colorizer .

Schier/ McArthur/ Vasulka Image Processor

This digital video processor contains a vertical interval control bus, gen-lock timing, and a microcomputer to orchestrate field by field control of the image. The digital video paths are connected to the processing modules through front panel patching permitting a variety of interconnections schemes. The components parts are :

1) A DEC LSI-11 microcomputer coordinating control words for processing and user interface functions.

2) A Vertical Interval Control Buffer LSI-11 Interface Control info. is loaded into the control buffer during the active field, for transfer to processing modules during the next vertical blanking interval. An interrupt is generated to the LSI-11 after the control buffer is transferred.

3) A Gen-Lockable Sync Generator - timing is based upon 512 H by 486 V active screen coordinates. Both video sync and Horizontal / Vertical timing is available on the control bus, for pickoff by modules.

Processing Modules :

A) Video Rate Analog to Digital Converters (A/D)

B) Selectors - 3 groups of selectors - choosing between 8 horizontal, and 8 vertical frame locked patterns, and an External digital video source. The selectors allow bit-wise selection of horizontal, vertical and input components.

C) Arithmetic Logic Units (ALU's) - Combines two digital input streams into a single output through combinations of arithmetic and Boolean logic functions. The Boolean functions of 'AND', 'OR', 'EXOR', 'EXNOR', Ones Complement are present. The arithmetic functions 'A PLUS B PLUS CARRY', 'A MINUS B PLUS CARRY', and 2's Complement are also available. Certain combination of arithmetic with logical operations are possible, with a 'Constant' available on the 'B' input, useful for bit masking.

D) Lookup Table - an R,G,B lookup table with common digital 'Address input' is present, to perform intensity/pseudo color transformations

E) Window generator - three Window generators, form an adjustable frame for gating/routing the digital sources. The 'Window Frames' are programmable on a pixel/line basis. Wipe patterns and title boundaries are formed here.

F) Digital to Analog Converters (D/A) - one apiece for red, green and blue channels.

G) RGB to NTSC color encoder - the final output is derived from the Red, green and blue components then converted to composite NTSC.

Input is received from camera sources, video tape or from the internal pattern generator (H and V timed bar patterns). Camera/VTR sources first go through the A/D converters, are front panel patched to the processing modules, route to the D/A's for conversion to Red green, and blue. The signals then hop into the RGB to NTSC encoder, converting to a composite NTSC video output, for display or further post-processing.

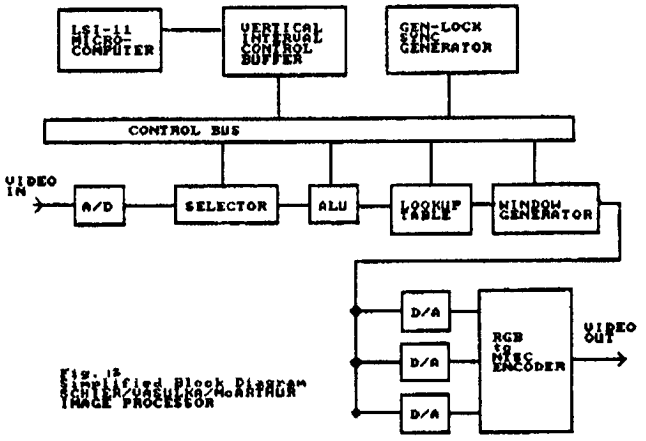

Fig. 12
Simplified Block Diagram
IMAGE PROCESSOR

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EIA RS170 (1957), RS-330 (1966), RS-343A (1969)
RS170A (tentative Nov. 8, 1977)

Vasulka Corporation
257 Franklin Street
Buffalo, N.Y.
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(716) 856 - 3385
Submitted by Jeff Schier

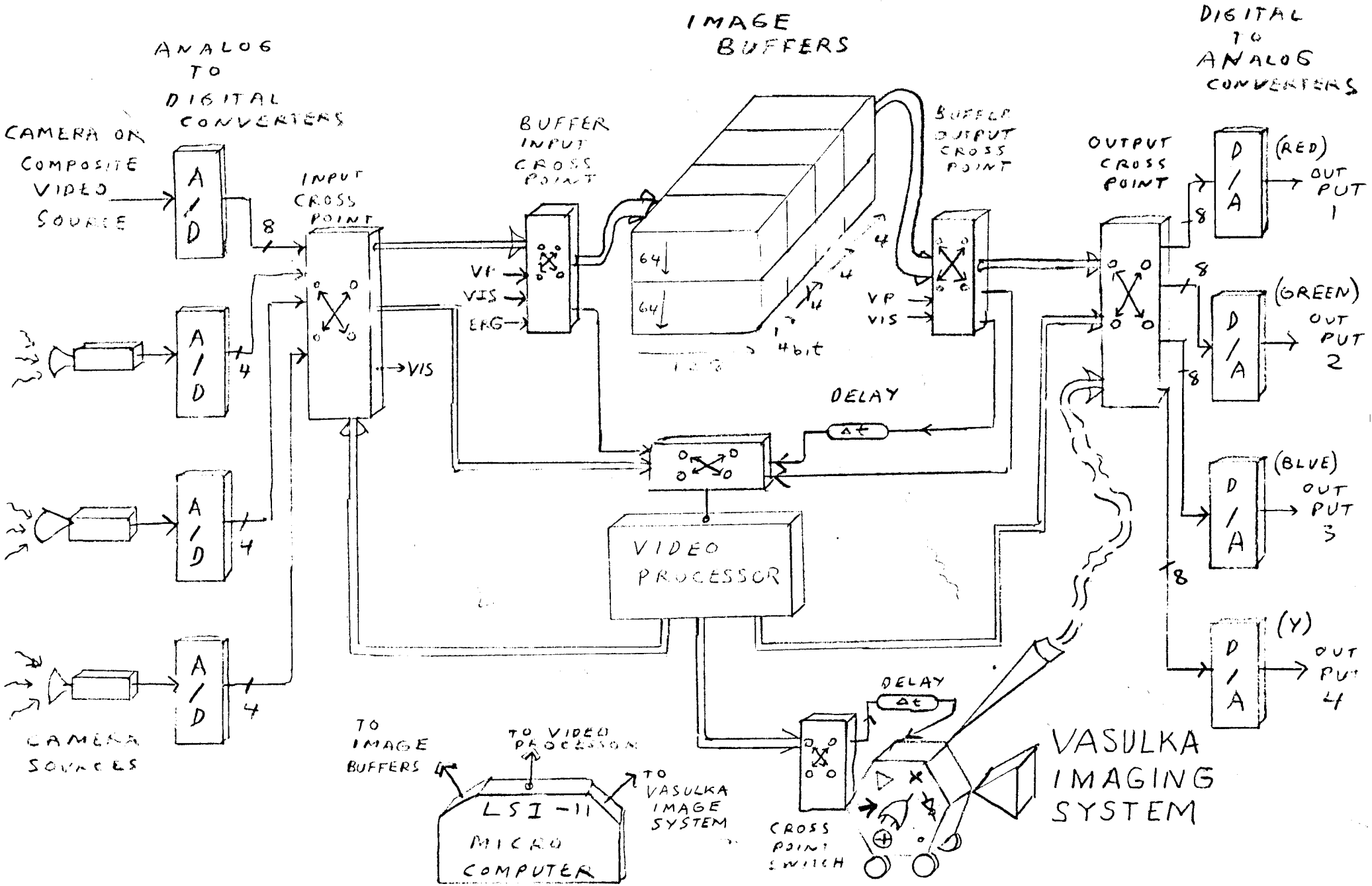
Dear Purchasing,

Below is a list of Packaging panels, and wire wrap accessories:

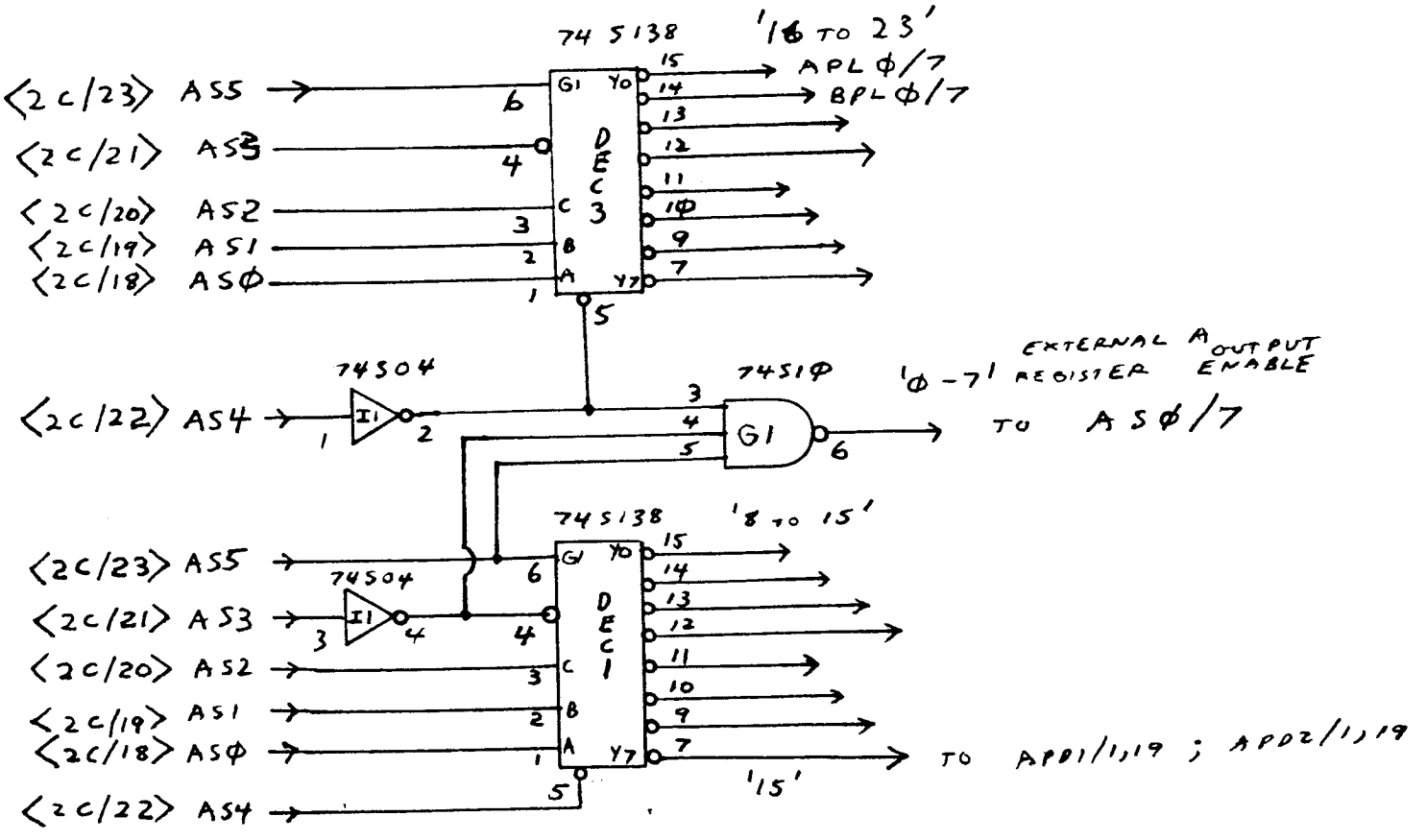
Mupac -

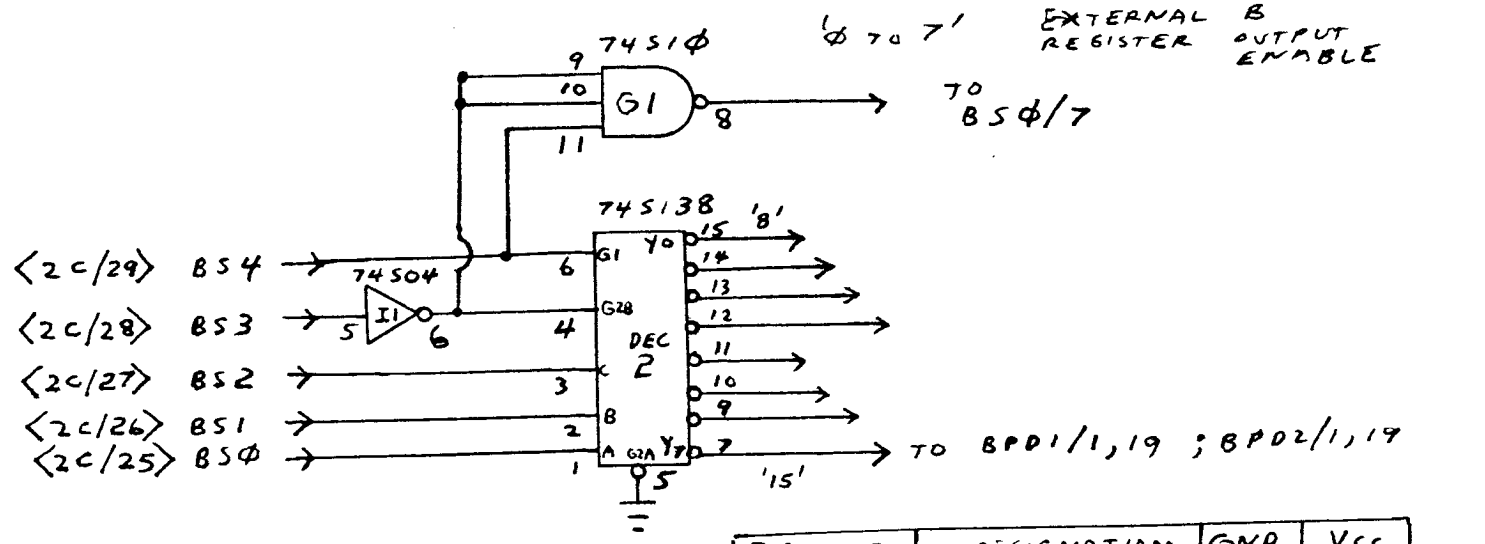
Quantity	Catalog 500 Number	Description	Unit Price	Total Price
1	3233080-01	Single width card extender		$ 129.25
1	3243080-01	Double width card extender		$ 199.00
1	3312549-03-02	"Mixer" Horizontal card rack 4/7 Panel rack, 12 connector Receptacles, Retma end plates, accomodates - two 326 panels two 324 panels, two 323 panels		$ 377.25
2	3264881-01	Triple width Universal panel without socket terminals	$109.00	$ 218.00
1	3245081-04	Double width "Sponge" panel without socket terminals		$ 75.00
1	3244881-01	Double width Universal panel without socket terminals		$ 75.00
2	3234881-01	Single width Universal panel without socket terminals	$53.00	$ 106.00
7	1301422-01	Socket terminals(100 pieces)	$11.90	$ 83.30
1	1301402-01	Socket terminals(100 pieces) (slotted)		$ 12.10
1	3752530-01	Socket terminal Insertion/extraction tool		$ 30.00
1	3611600-36	36 position receptacle (10 pieces)		$ 12.00
1	3611600-18	18 position receptacle (10 pieces)		$ 7.00
3	1311517-01	Mini terminal receptacle (100 piecs)	$15.40	$ 46.20
1	3752503-01	105CFM Fan		$ 39.95
		Mupac Total		$1410.05

BLOCK DIAGRAM - IMAGE EMULSIFIER



SELECTOR DECODERS





IC TYPE	DESIGNATION	GND	Vcc
74S138	DEC1, DEC2, DEC3	8	16
74SØ4	I1	7	14
74S1Ø	G1	7	14

Image Emulsifier
Ordering Information October 1978

Purchase Number	Description	Cost	Delivery
B12	Summit Distributors - EMI Filter and Miscillany	$ 19.60	Received
B13	C.K. Wall Sockets and Socket Terminals	$546.75	Received
B14	Summit Distributors - Ceramic Capacitors	$ 30.00	Received
B15	Summit Distributors - Capacitors	$ 54.00	Received
B16	Unused		
B17	Mupac - Rack and wire/wrap boards	$967.60	RECEIVED
B18	Samtek - Sockets and Socket terminals	$370.50	Received
B19	Summit Distributors - Semiconductors	$ 30.00	Received
B20	Schweber Electronics - Semiconductors	$175.75	Received
B21	Hamilton Avnet - Assorted Semiconductors	$278.64	
B22	Summit Distributors - Solder tail sockets	$ 29.20	Received
B23	Unused		
B24	Hamilton/Avnet - Semiconductors, data selectors	$ 57.80	
B25	Hamilton/Avnet - Semiconductors, assorted	$ 25.95	
B26	Summit Distributors - Semiconductors	$ 53.25	Received
B27	Summit Distributors - Interface Semiconductors	$ 16.11	Received
B28	Cramer Rochester - Schottky Ics	$101.26	

Page Total $ 2756.41

Total $ 7651.96

Ordering - Image Emulsifier

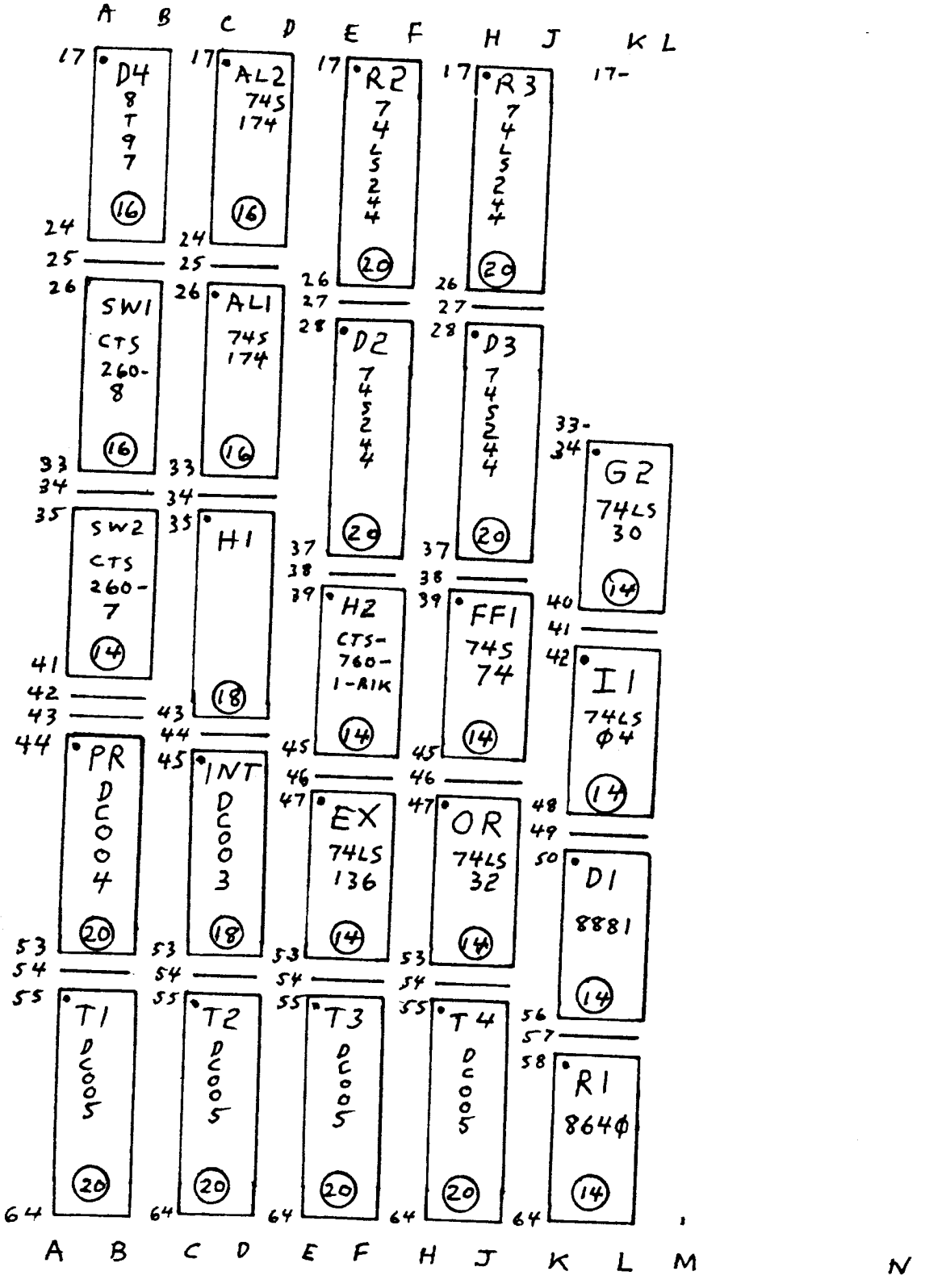
August 8th, 1978
Jeffy Schier

Purchase Order #	Description/Company	Cost	Received?
B - 01	Digital Equiptment Corporation LSI-11 Interface - DCK11-ac	$ 176.25	Yes
B - 02	Powermate SW - 5 - G Power Supply	$ 265.00	Yes
B - 03	OK Wire and Tools Wire Wrap tools	$ 185.74	Yes
B - 04	Mupac - Packaging and Wire Wrap panels	$1390.30	Yes
B - 05	Harvey Federal (Rochester) Buffer memories (Intel P2141-2)	$1554.30	Yes
B - 06	Hamilton Avnet Assorted Semiconductors	$ 384.40	
B - 07	Rochester Radio Semiconductors/Memories	$ 240.60	Yes
B - 08	Data Delay Devices Delay Lines	$ 52.00	Yes
B - 09	Hamilton Avnet Control Store Memory (93L422)	$ 436.80	
B - 10	Unused		
B -11	Schweber Electronics Arithmetic Logic Units	$ 210.16	Yes
	Total 8/8/78	$4895.55	

LSI-11 INTERFACE - LAYOUT

Jeffry Lehman

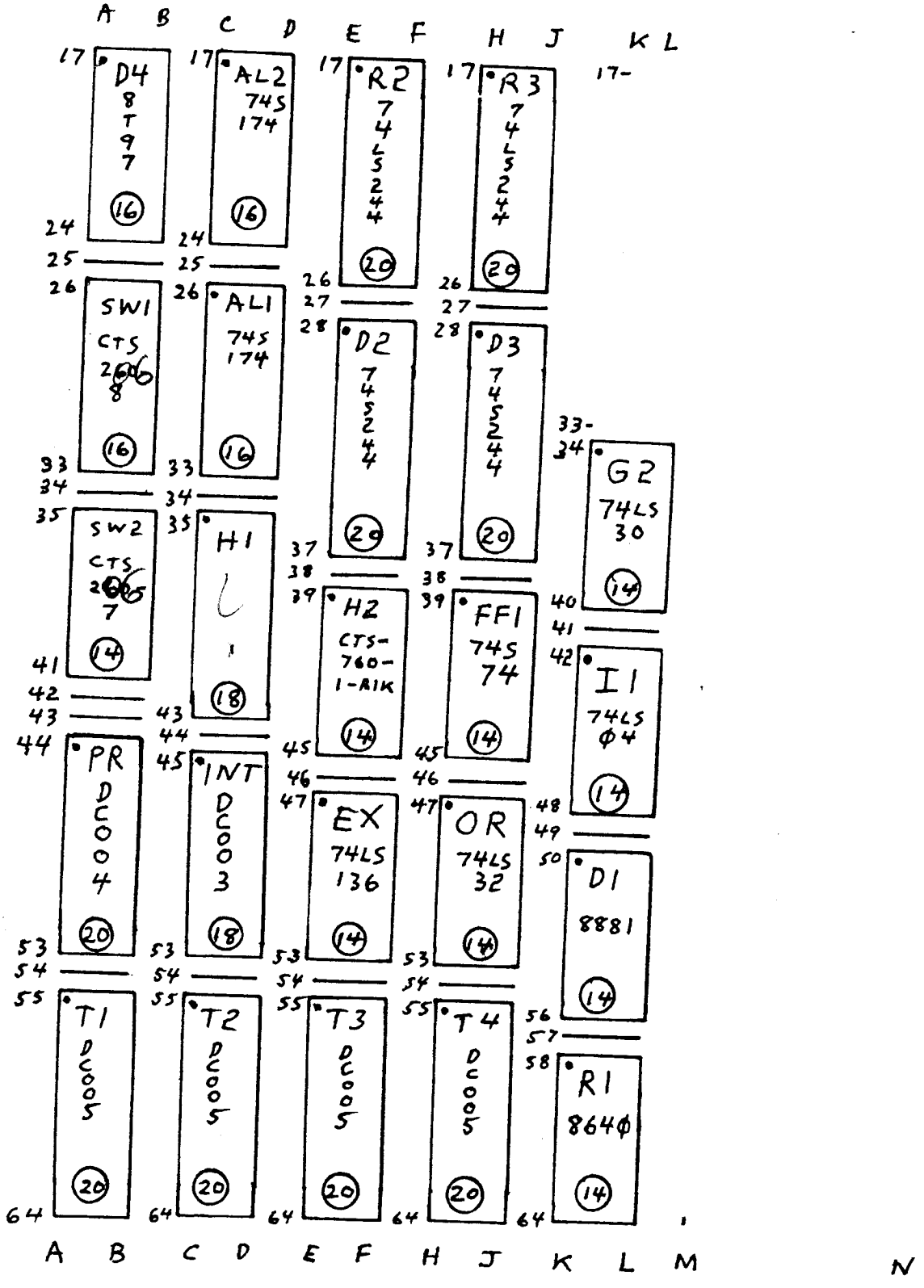
COMPONENT / WIREWRAP SIDE

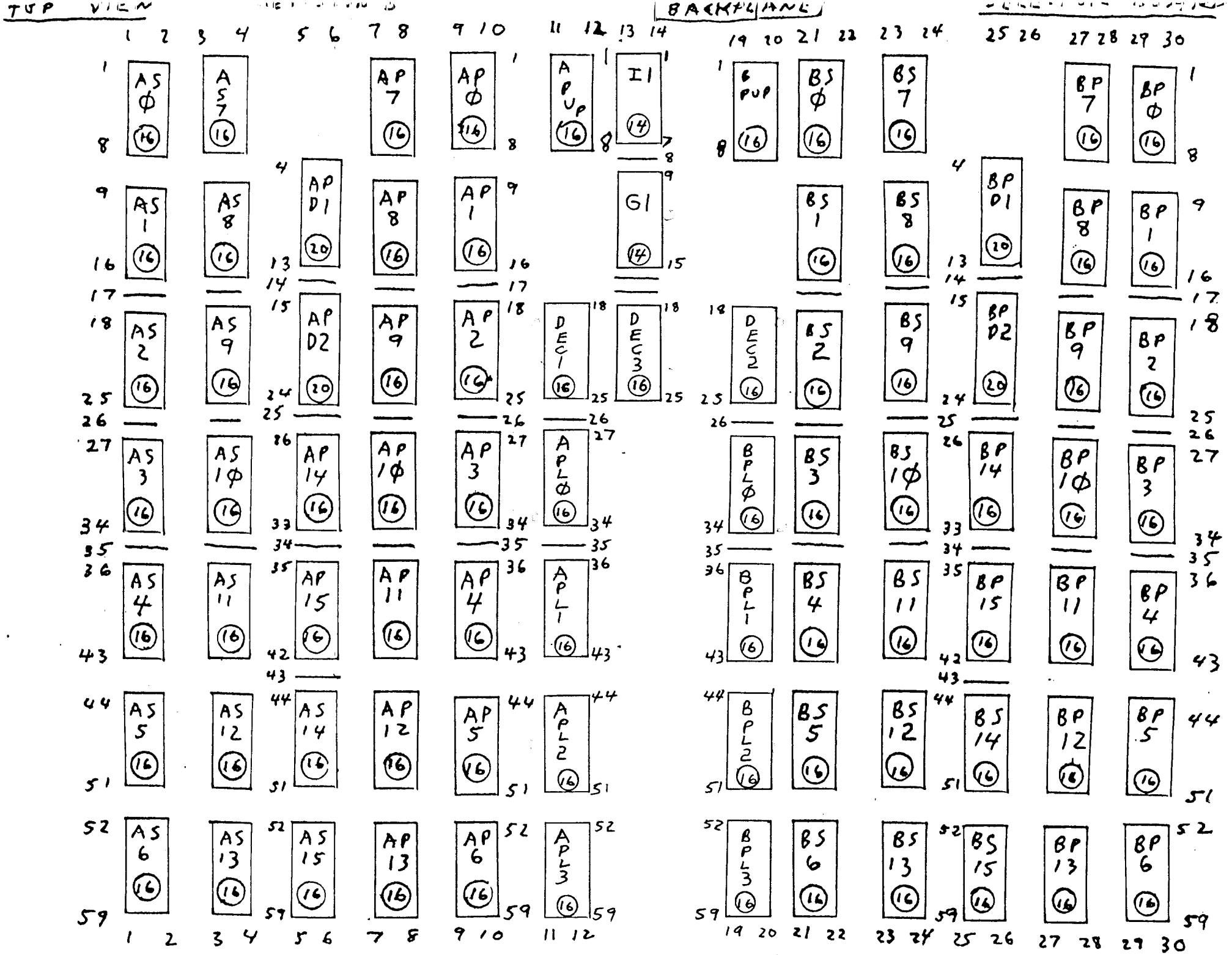


LSI-11 INTERFACE - LAYOUT

Jeffrey Johnson

COMPONENT / WIREWRAP SIDE




TOP VIEW
BACKPLANE
AS Φ 16
AS 7 16
AP 7 16
AP Φ 16
AP UP 16
I1 14
BP UP 16
BS Φ 16
BS 7 16
BP 7 16
BP Φ 16
AS 1 16
AS 8 16
AP D1 20
AP 8 16
AP 1 16
G1 14
BS 1 16
BS 8 16
BP D1 20
BP 8 16
BP 1 16
AS 2 16
AS 9 16
AP D2 20
AP 9 16
AP 2 16
DEC1 16
DEC3 16
DEC2 16
BS 2 16
BS 9 16
BP D2 20
BP 9 16
BP 2 16
AS 3 16
AS 10 16
AP 14 16
AP 10 16
AP 3 16
APLΦ 16
BPLΦ 16
BS 3 16
BS 10 16
BP 14 16
BP 10 16
BP 3 16
AS 4 16
AS 11 16
AP 15 16
AP 11 16
AP 4 16
APL1 16
BPL1 16
BS 4 16
BS 11 16
BP 15 16
BP 11 16
BP 4 16
AS 5 16
AS 12 16
AS 14 16
AP 12 16
AP 5 16
APL2 16
BPL2 16
BS 5 16
BS 12 16
BS 14 16
BP 12 16
BP 5 16
AS 6 16
AS 13 16
AS 15 16
AP 13 16
AP 6 16
APL3 16
BPL3 16
BS 6 16
BS 13 16
BS 15 16
BP 13 16
BP 6 16

10-30-78

THE VASULKAS
257 FRANKLIN ST.
BUFFALO, N. Y. 14202
716-856-3385

February 10, 1976

... Equipment Corporation
... Pinton Hills
... Park - Fairport
Rochester, New York 14450
Att: Paul Gizzi

Dear Sirs:

I am interested in purchasing the following equipment from you:

1	RXV 11 - BA		$3900.00
1	RX01K - 10		75.00
		Tax 7%	278.25
		Total	$4253.25

Would you kindly notify me as to what billing procedure will be necessary? Thank you for your kind attention to this matter.

Sincerely,
Bohuslav Vasulka (msd)
Bohuslav Vasulka

BV/msd

DIGITAL IMAGE PROCESSING

Thomas W. Moxon
EE 499 - Work Study Program
Professors:
Woody Vasulka
David Bennenson

The subject of my independent study this semester has been the theory and methods of digital image processing. Digital image processing is the term applied to the numeric codification and subsequent algorithmic manipulation of pictorial information.

This codification, or quantization, of the image is performed on a point by point basis as the picture is scanned, where each point is assigned a number corresponding to the luminance value of the picture at htat point. The range of numbers that may be assigned to each point determine the amount of discrete intensity changes that may be detected; while the number of individual points determine the smallest area of the picture that may be encoded. This quantization is normally implemented with a television camera and analog - to - digital conversion circuitry; where the digital word size corresponds to the range of numbers which may be assigned, and the analog sampling rate determines the number of individual points that may be resolved from the original picture. I will expand on these concepts in the section on quantizers.

The digital processing of the scene content however, tends to follow two different paths, that of pipeline processing and that of storage, or frame buffer processing. Pipeline processing is, as the name implies, a method where an operation is performed upon the scanned stream of picture elements as they are passed to the output display or recording unit, in a continuous fashion. The main advantage of this method is the high speed with which operations may be performed, allowing the capacity for real-time motion within the frame. However, since the frame exists only as a continuous stream of picture elements, hereafter refered to as pixels, there is no capability for operations which require knowledge of, or comparision with, past scene information.

Examples of operations that may be performed with pipeline processing are color mapping, intensity remapping, window formation and digital keying.

Frame buffer processing is the term applied to the storage of single frames, or sequences of frames; allowing transformations of pixel location within a frame, or over a number of frames. This method gives the capability of performing operations which are time variant, such as compression and expansion of the image, trajectory tracing, and pattern recognition. It's main disadvantage though, is the extremely slow speed of storage and recall, resulting from the sheer volume of data involved. Most image processing systems encorporate both methods, under computer control, to achieve a wider variety of operations. The "Image Emulsifier" , which I have been helping the Vasulka Corp. to develop this semester, is just such a system.

Description of the Image Emulsifier

The Image Emulsifier system is a microprogrammable processor for the aquisition,storage,modification,and distribution of digitally encoded images of four bit resolution. The system currently consists of the following subsections:

]) Quantizers- Two high-speed analog- to -digital converters operating on separate buses are employed for the real-time aquisition of two camera images by the system. I constructed and tested the quantizers, which are based around the new Advanced Micro Devices 6688 integrated circuit.

2) Image Buffers- Eight image buffers of 8k deep by four bits wide with high-speed access (200 nanosecond) time. Entering each buffer are four busses carring control signals,address and data information. At any time, any buffer may be connected to any one of the four busses. This allows for expansion of the image resolution by concatenation of several buffers onto the same bus; for example, connecting two buffers to the "A" bus makes them appear to the bus as a widened, 8K by 8 bit buffer. Connection of a particular buffer to a bus is initiated by the buffer priority logic, associated with each buffer. I constructed four of the eight image buffers, and am in the process of testing them at this time.

3) Microprogrammed Microprocessor- A high-speed (200 nanosecond) microprocessor is connected to two of the four busses fed to the image buffers. By controling two busses, reading or writing may be done to different locations in two different buffers. This gives the capability of variuous picture transformations, such as picture inversion, compression, expansion, edge extraction, and outlining. A 3K program control store and sequencer gives instructions to the microprocessor, which is structured around an 80 bit pipeline. This control store has the capability for expansion which will allow Prommed, or hardware stored programs to be permenently resident in the memory, to facilitate execution of the most commonly used microprograms. The microprocessor is based on the Advanced Micro Devices 2900 series of integrated circuits, which employ the latest method of microprocessor design, that of the Bit Slice concept.

4) Microcomputer Interface- The particular interface involves connection of the Image Emulsifier to an LSI-11 microcomputer. The interface connects the LSI-11 to the microprocessor and to one bus of the buffers. A buffer request register is on the interface, to allow requests for usage of a particular buffer. To access the data of a buffer, the LSI-11 must first request usage; if it is the highest priority device, a grant register will indicate that it has usage of the buffer. This grant register can be enabled to generate interrupts, upon getting the buffer that was requested. Once a request/grant sequence is successful, a 1K block of data may be written to, or read from, the granted buffer. To write to other sections of the buffer a memory page register is used, to map the 1K memory space into one of the pages of the 8K buffer.

The LSI-11 is also responsible for setting the buffer priority registers on the eight image buffers. The LSI-11 must monitor the buffer activity, to time the change of priorities which affects the next memory cycle of the buffers. The LSI-11 is also responsible for loading the control store of the microprocessor, and has various control registers to facilitate this operation. It controls the run/single step/stop of the microprocessor to allow debugging of the microprograms, and serves as the main memory for controling programs. At the present time we are implementing an assembler/disassembler to ease the task of microprogramming the Image Emulsifier.

5) Buffer and Screen Addressing Circuitry- This section accommodates the generation of the horizontal and vertical timing to scan out, or write in, digitized video information to the image buffers. This will allow such effects as adjustment of the height and width of the picture, shifts of the position on the screen, and various pixel position remappings.

A preliminary constraint is to lock the phase of the high frequency clock to the video subcarrier phase, to avoid color shifts in the system. The timing of the X-Y timing chain , determining the pixel coorinates, is in turn locked to this high frequency clock. The high frequency clock itself sets the 'time grid' which specifies the maximum and minimum resolution attainable in the scanning of the buffers. With a high frequency clock of 9.75524 MHz and an active video line of 52.4 microsecond duration, this forms a total number of 512 picture elements as the maximum resolution of the system. However, due to the buffer cycle time of 200 nanoseconds the resolution is further limited to 256 pixels as the maximum. Thus,to store a 256 by 256 image requires some 65,536 memory locations, which is just the size of our complete buffer memory. By using all eight buffers simultainously one frame of 256 by 256 resolution may be stored, but more frames may be stored simultainously if a lower resolution is used. For instance, if 128 by 128 resolution is used then 4 frames may be stored at one time, and if 64 by 64 resolution is used then 8 frames may be stored. A control register is employed to indicate the desired resolution mode of the buffers, which adjusts the timing logic accordingly.

A mapping memory of 256 words by 8 bits is placed on the output of the X-Y address timing , one for the X and one for the Y addressing. These memories may be loaded with a function, which will translate the

sequential X and Y into a different addressing scheme. These memories can be loaded during the inactive scan and utilized during the next active scan.

The use of high speed multipliers on the X-Y signals is another possiblity for image transformations. A 200 nanosecond multiplier of 16 bits width is employed on one bus to facilitate the loading of maps with transformations, or to use directly on the image data itself. In instances where transformations require pixels to be skipped or discarded, such as image compression, one places the task of which pixels to be skipped upon the round off error of the multiplier itself.

For more random addressing or data generation, a pseudo-random number generator has been implemented, with a variation on the shift register that allows the next input to be determined from the addition of selected bits of the register. This gives repeating sequences of programable length. However, by loading the register directly from the X-Y clock an unlocked noise source is then generated, due to the mismatch of the pseudo-random sequence to the video line/field blanking rate.

My role in this section of the system has been the design and construction of the phase locked loop for the high frequency clock, and testing of the address counters and maps. The multiplier circuit remains to be wired and tested, possibly this week.

6) Output Selection Logic- The output selection logic is responsible for routing the buffer outputs and other units to one or more of the four outputs of the system. A screen addressing unit further segments the outputs into four quadrants, according to the cartesian coordinate system.

(CORRECTED VERSION (BY JEFFY AND STEIML)

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IMAGE

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ONCE GRANTED, THE BUFFERS ARE ACCESSED THROUGH A 1K ADDRESS 'WINDOW'. TO READ/WRITE THE FULL 8K BUFFER, AN EXTENDED ADDRESS REGISTER (PAGING REGISTER) IS USED TO SHIFT THIS WINDOW OVER EIGHT 1K BUFFER SEGMENTS

5) Buffer and Screen Addressing Circuitry- This section accommodates the generation of the horizontal and vertical timing to scan out, or write in, digitized video information to the image buffers. This will allow such effects as adjustment of the height and width of the picture, shifts of the position on the screen, and various pixel position remappings.

A preliminary constraint is to lock the phase of the high frequency clock to the video subcarrier phase, to avoid color shifts in the system. The timing of the X-Y timing chain , determining the pixel coorinates, is in turn locked to this high frequency clock. The high frequency clock itself sets the 'time grid' which specifies the maximum and minimum resolution attainable in the scanning of the buffers. With a high frequency clock of 9.75524 MHz and an active video line of 52.4 microsecond duration, this forms a total number of 512 picture elements as the minimum resolution of the system. However, due to the buffer cycle time of 200 nanoseconds, the resolution is further limited to 256 pixels as the maximum. Thus,to store a 256 by 256 image requires some 65,536 memory locations, which is just the size of our complete buffer memory. By using all eight buffers simultainously one frame of 256 by 256 resolution may be stored, but more frames may be stored simultainously if a lower resolution is used. For instance, if 128 by 128 resolution is used then 4 frames may be stored at one time, and if 64 by 64 resolution is used then 8 frames may be stored. A control register is employed to indicate the desired resolution mode of the buffers, which adjusts the timing logic accordingly.

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~~My role in this section of the system has been~~ the design and construction of the phase locked loop for the high frequency clock, and testing of the address counters and maps. ~~The multiplier circuit remains to be wired and tested, possibly this week.~~

6) Output Selection Logic- The output selection logic is responsible for routing the buffer outputs and other units to one or more of the four outputs of the system. A screen addressing unit further segments the outputs into four quadrants, according to the cartesian coordinate system.

A sixteen section control register dictates the unit to be output in each quadrant of all four system outputs, allowing a single unit to be displayed on the entire screen or to segment the screen into a maximum of four areas, with a different unit being displayed in each area. ~~The output unit can also key, or switch point by point between two separate units (images).~~ A use of these features might be the simultainous acquisition and display of four separate camera images, with a program running on the microprocessor that compares past and present frames of each camera to detect motion in front of any camera, blinking in red any area in which motion occurs.

7) Digital -to-Analog reconversion- This section of the system will reconvert the four bit digital outputs into a lvp-p ~~composite~~ video signal, ~~complete with sync and blanking. These four identical units remain to be constructed, and this will be part of my work this summer.~~ Based on the Analogic 8038 hybrid converter, the units will feed a standard color encoding unit (R,G,B or C C B Y), which accepts red,green,blue, and luminance signals to form a composite color video signal, ~~of recordable quality.~~

In conclusion, I think the work I was involved in this past semester was immensely rewarding, giving me invaluable experience in image processing, as well as high frequency digital circuits and techniques in computer interfacing and control. This work was excellent background for my major in Electronic Arts, as aesthetic, as well as technical considerations, all had to be weighted equally.