Returning to the A B C counters, note another important feature of the design, that each counter is loaded with the output of the succeeding counter. A is loaded by HD from B which is loaded by VD from C. This establishes synchrohous video operation. A is known as the pixel or warp counter, B is the line or weft counter, and C is the frame counter.

Clock signals for each counter are derived through variable modulo counter dividers N, FL, and D. These are 74193 type circuits. Counter N is fed with Ø clock pulses and its divided output clocks counter A. The N counter must also be reset at the beginning of each scan line, which is accomplished by wired OR of HD at its LOAD input. In similar fashion, HD is fed to counter FL as clock and its divided output clocks counter B. The FL counter is reset at the beginning of each field by VD. Counter D is fed with frame pulsesand its divided output clocks counter C.

The divider counters are jam loaded from identical counters functioning as latches to establish the divider modulus, (N), (FL), and (D). The value of these numbers determine respectively the warp size, weft size, and frame rate or speed of animation. Put another way, the warp size is the dimension of horizontal element and the weft size is the number of scan lines in vertical dimension.

The latches are loaded with values from the data bus via instruction decoder. An additional latch (C) loads data into the C counter under instruction command, and also supplies two bits to select the page in RAM under consideration for writing.

RAM is 256 bits in 4 pages of a 1K static MOS memoery. The 8 bits are fed by the outputs of counters A and B as address, with a cursor pulse controlling write mode at a specified coordinate, and instruction decoder control for fill or erase. Though only one RAM is shown, in practice 3 RAM planes are used to generate one bit for each color RED,GREEN,and BLUE; this provides 8 colors. More RAM planes would supply additional color but other techniques can be used to map 8 codes into many user selected colors.

By raising the A and B clock rates sufficiently, and employing folding signals to the BNA and DNB these few bits of RAM can be expanded into a fine resolution display on the screen. For example a playing court need only be entered into RAM in ½ or 1/8 size with memeory expansion through reflection used to generate the full court. ROM could be used in place of RAM to form "players" in a mode different from the "Video Etch-A-Sketch described above.

Though shown as a four bit system, this concept is readily expanded to 8 bits or more for more resolution. The video warp and video image outputs are resistively matrixed into video R,G,B, or I,Q,Y, modulation in the encoder circuit.

Beck Digital Video Weaver

A "Visual Processor" for Color Television Display

by Stephen Beck

The analog between a traditional loom and modern television display struck me as so obvious that in early 1974 I designed an all digital video synthesizing circuit named the video weaver. TV displays with scan lines running horizontally across the screen and stacked vertically to form a two-dimensional raster correspond exactly to the weft and warp structure of woven textiles. The warps of a loom correspond to pixels or elements of a video scan line, while the wefts of a loom correspond to the individual scan lines forming the raster.

Applying this realisation to a circuit in digital form, and 18 months of subsequent design and refinement result in my video weaver circuit, which uses primarily three types of TTL IC logic, NAND gates, D type flip flops, and programmable up/down counters. The addition of a decoder, data and instruction busses, RAM, and 12 pushbuttons comprise a powerful image processor, which feeds a video encoder circuit to produce a standard color TV signal.

With an additional cursor circuit, distinct pictures can be woven in color, and additionally be animated according to several basic image algorithms, move up, down, diagonally, zoom, scale by stretch or squeeze, etc. In addition, the circuit supplies many audio frequency signals which can provide a sound dimension to the display.

Since any video signal generator requires horizontal and vertical synchronizing pulses, and a 3.58 MHz subcarrier signal for color, the video weaver utilizes these pulses for all its operations.

Refering to the video weaver schematic, each drive pulse and the subcarrier sine wave (HD, VD, & ϕ) are capacitively coupled to biased, Schmidt trigger NAND gates. Input impedance is several K ohm, signal amplitude is 2-4 volts, and the resultant out-out pulses are then at TTL logic level. The VD 60 Hz pulse is also fed to a flip-flop and divied by 2 to produce a 30 Hz frame pulse.

One important part of this design is a series of cascoded counters A,B,C. These are up/down synchronous counters with jam load data inputs. Each counter if fed by a quad NAND gate steering array, which controls counter RUN/HOLD and UP/DOWN modes. These modes (RNA, DNA, RNB, DNB, RNC, DNC) are set internally by bits in a latch composed of D-type flip-flops.

A data bus controlled by pushbutton switches and an instruction decoder controlled by pushbutton switches perform all control operations. For example, the counter modes are set by loading the MSB of DATA bus into latch flip-flop activated by the decoder